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RESEARCH ON FPGA BASED EVOLVABLE HARDWARE CHIPS FOR SOLVING SUPER-HIGH DIMENSIONAL EQUATIONS GROUP

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Abstract. Solving a super-high dimensional equations group is widely used in science and engineering, but the slow solution speed is the biggest problem researchers face. Research on FPGA based evolvable hardware chips for solving the super-high dimensional equations group (SHDESC) is proposed in this paper. These chips can be implemented on a milliongate scale FPGA chip. The core architecture of SHDESC is a systolic array which consists of thousands of special arithmetic units and can execute many super-high dimensional matrix operations parallelly in short time as well as really achieve the purpose of high speed solution in hardware/software codesign. The experiments show that these chips can achieve high precision results in a short period of time to solve a super-high dimensional equations group.

Key words. Evolvable Hardware, Super-High Dimensional Equations Group, FPGA, Hardware/Software Codesign, Systolic Array

1. Introduction

Solving a super-high dimensional equations group is widely used in science and engineering, for instance, in optimization structure of oil wells and mining, structural analysis of mineral resources, calculation of deformation of bridges and housing construction after the force, computation of the flow field around the aircraft in aerodynamics, and evaluation of the flow of the atmosphere in weather forecast. These problems are transformed into a super-high dimensional equations group to solve ultimately. The process of solving these problems is described by a number of differential equations. In general, solving these differential equations is acquiring a super-high dimensional equations group which has thousands or even millions of unknowns after discretizing differential equations, no matter whether the difference method or finite element method is used. Thus the advantages and disadvantages of a method to solve the super-high dimensional equations group are restricted to solving these problems largely. To find an efficient, fast algorithm to solve a super-high dimensional equations group, many scholars continue to carry out in-depth and long-term studies[1]-[5].

With the advances in modern microelectronic technology, The EDA technology has developed greatly in every aspect. One of this technology is evolvable hardware [6][7] which uses an intelligent, self-reproduction and self-healing method to design hardware. It refers to hardware that can change its architecture and behavior automatically and dynamically through interacting with its environment, which can be presented in the formula [7]: Evolutionary Algorithm + Programmable Logical Devices = Evolvable Hardware.

Research on FPGA based evolvable hardware chips for solving a super-high dimensional equations group (SHDESC) is proposed in this paper. This method is

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researched on solving the super-high dimensional equations group with the evolvable hardware theory and hardware/software codesign technology, and implemented on a million-gate scale FPGA chip. The bottleneck of slow speed is mainly concentrated on the super-high dimensional matrix operations in the process of solving the super-high dimensional equations group using traditional algorithms. But the chips are implemented on a million-gate scale FPGA chip, and its core architecture is a systolic array which consists of thousands of special arithmetic units that execute matrix operations concurrently, break through the bottleneck of slow solution speed, make super-high dimensional matrix operations in a short period of time, and really achieve the purpose of hardware/software codesign to solve with high speed. On the one hand, this chip combines the advantages of evolvable hardware, which are intelligence, efficiency, and parallelism. On the other hand it makes full use of the advantages of modern VLSI, which are high integration, low cost, and easy to achieve the operation of parallel computing. Therefore, it improves the speed of solving the super-high dimensional equations group greatly and really achieve the purpose of hardware/software codesign to solve with high speed.

2. Design Process of FPGA

The designing process of FPGA (Field Programmable Processor Arrays) is the process of using EDA development software and program utilities to develop FPGA chips. The development process of FPGA includes design of function circuit, design entry, function simulation, synthesis optimization, simulation after synthesis optimization, system implement, circuits and wires distribution, time sequence simulation and verifying, circuit board level simulation and verify, and programming of Soc (System of chip) and verifying[8][9].

2.1. Design of Function Circuit. Before system designing, some preparations such as schematic verifying and the selection of FPGA chip have to be done. Then the complexity of the indexes in system, running speed of FPGA, resources provided by chips and cost should be analyzed according to the requests of projects. After that, reasonable design schedule and suitable types of devices have to be selected; and at last the design method from top to down is used in general in the world. In this method we partition the circuit system to some base units as a top layer, and partition every unit to next base unit of next layer and so on, until we can find and load the EDA components from the components library to construct the complete circuit of the project.

2.2. Design Entry. The goal of design entry is to demonstrate the circuit system according to the requests of software development, and design entry is a process for input program to EDA utilities, and for input the components loaded from circuit components library to the circuit system using software or other design utilities. These software or design utilities are the main design utilities of EDA of FPGA, such as hard description language (HDL), Handle-C language and utility of schematic diagram description.

2.3. Function Simulation. Function simulation is called pre-simulation. Namely, function simulation is to verify the logic function of circuit system designed by using HDL programs before compiling the HDL programs, and this function simulation doesn't include the verification of delay circuits. In the first place, we use wave editor and HDL to build wave file and verified vector (namely, combining input signals to a execution sequence), and then the results will be saved in a report file and output signal waves which show the signals' change of all the circuit notes.